APPLICATIONS OF THE SILICON PLANAR II MOS FET

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E. R. deAtley, Technical Writer and Editor

I. INTRODUCTION

The FI100 Metal Oxide Silicon Field-Effect Transistor (MOS FET) is the first of a new line of products manufactured by a refined planar process known as PLANAR II. In earlier planar MOS FET's the dielectric was subject to charge migration due to heavy electric fields (up to 1 million volts per centimeter) often met in operation. This charge migration caused gross changes in device operating parameters and deterioration of P-N junctions. The PLANAR II MOS FET, however, can withstand electric fields of the order of 2 million volts per centimeter without dielectric charge migration and therefore is an inherently stable device.

This note describes the physical characteristics of the PLANAR II MOS FET and gives a number of applications made possible by the special properties of this device.

II. PHYSICAL CHARACTERISTICS

Figure 1 is a cross-sectional representation of the MOS FET showing DC biasing polarities. Two P islands are diffused close together into a high-resistivity N substrate and covered by a thin insulating layer of silicon dioxide (stipled area in the diagram). Metal electrodes called the "source" and the "drain" are evaporated in the oxide layer in contact with the P islands. A third metal electrode called the "gate" is evaporated on the oxide layer insulated from the source and drain, and a fourth—the "base substrate"—is connected at the bottom of the N-type material.

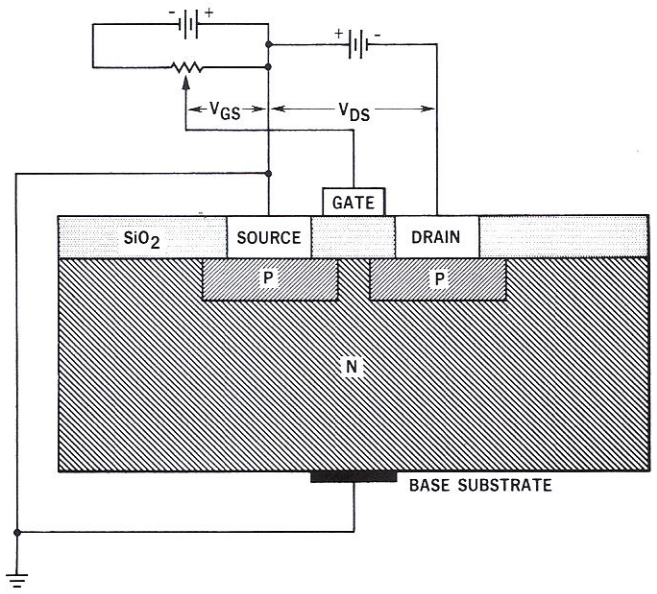

Fig. 1. Cross-section of MOS FET with correct biasing polarity.

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A negative potential (V_{GS}) applied between gate and source repels electrons from the N-type channel immediately below the oxide layer and attracts holes. As V_{GS} is made more negative, the N-type channel between the P islands is finally converted to P type and current flows from source to drain. The gate potential at which current begins to flow is called the gate threshold voltage, V_{GST}. Further increases in V_{GS} beyond V_{GST} widen the channel and increase current flow. No current flows in the gate, however, because of the insulation provided by the oxide layer.

Figure 2a shows an equivalent small-signal circuit† of the Fairchild FI100, which is fairly accurate to at least 20 Mc. The electrical symbol of the device is shown in Fig. 2b.

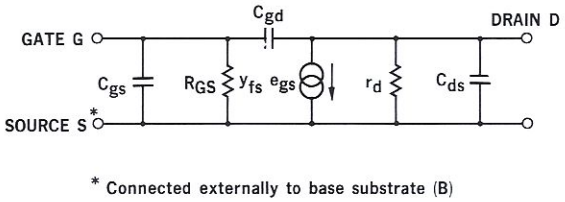


Fig. 2a. Small signal circuit model.

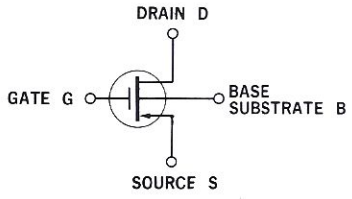


Fig. 2b. Electrical symbol.

The FI100 is a transconductance device similar to a pentode except that its transconductance is lower. It has an unusually high input impedance ($>10^{13}$ ohms). In fact it compares very favorably with the electrometer tube, having better drift characteristics and warm-up time.

The device operates in what is called the "enhancement mode" because a certain minimum gate voltage V_{GST} must be applied to cause conduction. The FET, on the other hand, is called a "depletion-mode" device because it requires a voltage to turn it off. The MOS FET can be made in either the enhancement mode or the depletion mode, but the enhancement mode has the advantage that it can be "self-biased," as explained below.

III. DC OPERATING CHARACTERISTICS

Figure 3 shows characteristic curves of the drain voltage V_{DS} versus drain current I_D, with gate voltage V_{GS} as a running parameter. The dashed-line curve is the locus of points at which $V_{GS} = V_{DS}$. At any point on this curve the drain and gate can be connected without DC current flow between the two because the two points are at the same potential and the gate is insulated from the source-drain circuit by the silicon-dioxide layer. Thus the size of the resistance between the gate and drain will have no effect on operating conditions.

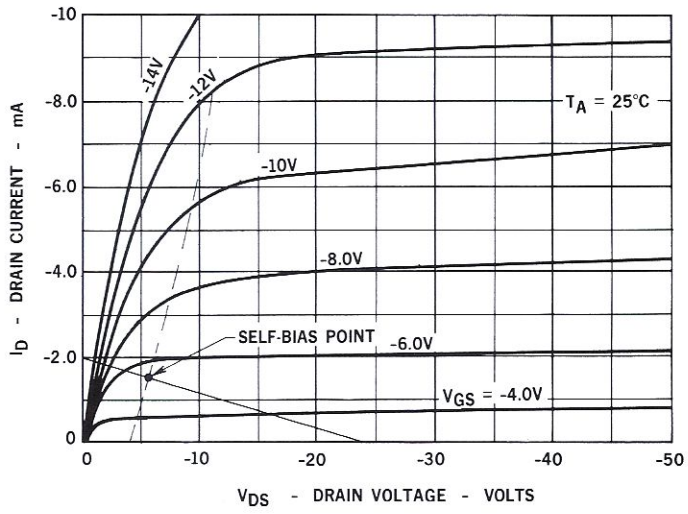


Fig. 3. FI100 drain characteristic curves with 2.4 K load line and locus of VGS = VDS points superimposed.

†Symbols used in the equivalent circuit and elsewhere in this note are defined in the List of Symbols at the end.

If a load line is superimposed on the curves in Fig. 3 to represent a given value of drain load resistance, the intersection of this load line with the $V_{GS} = V_{DS}$ curve will be a "self-bias" operating point. This can be shown with an example.

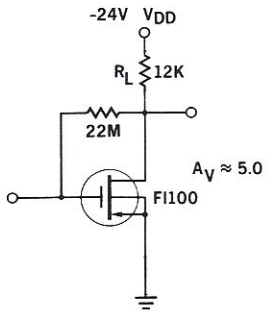


Fig. 4a. Self-bias circuit.

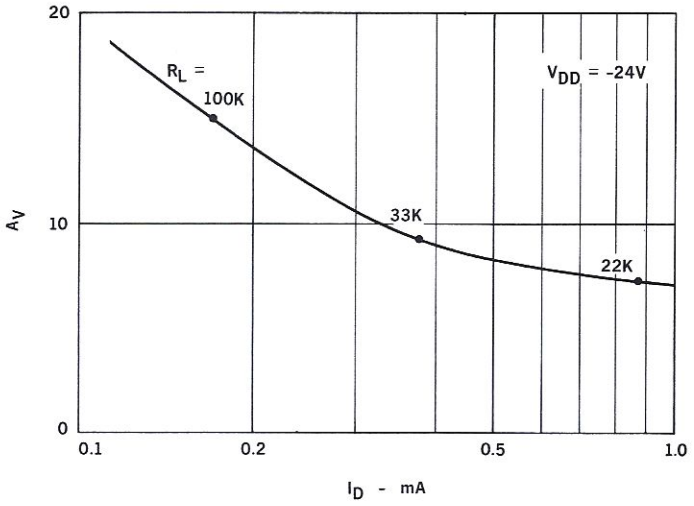


Fig. 4b. Voltage gain versus drain current for various values of load resistance.

Suppose that a supply voltage V_{DD} of -24 V and a load resistance R_L of 12 K are chosen, as shown in Fig. 4a. The load line for these conditions plotted on the drain characteristic curves of Fig. 3 intercepts the $V_{GS} = V_{DS}$ curve at 5.5 V. At this operating point the dynamic output resistance r_d can be calculated to be 100 K and the transconductance y_{fs} is 600 μmhos. Neglecting the 22 M feedback resistor, we obtain the calculated voltage gain A_v as follows:

$$A_v = \frac{y_{fs} r_d R_L}{r_d + R_L} = \frac{600 \times 10^{-6} \times 100\,K \times 12\,K}{112\,K} = 5.4 \qquad (1)$$

Figure 4b represents graphically the relationship between A_v, R_L, and I_D.

The input resistance R_{in} is given by the relation

$$R_{in} \approx \frac{R_f}{A_v} \qquad (2)$$

The feedback resistance R_f can be as large as 10^{15} ohms, but for this example we have chosen 22 M. The input impedance will therefore be about 4 M shunted by C_{gs} and $C_{gd} \times A_v$.

It is apparent from Eq. (1) that the rather low transconductance of the FI100 makes it necessary to use a large value of R_L for maximum voltage gain. However, the transconductance—and therefore the voltage gain—can be increased by the simple addition of a transistor emitter-follower, as shown in Fig. 5.

The emitter-follower is easily diffused into the MOS FET integrated circuit and involves no problems of interaction. In effect the transconductance of the MOS FET is multiplied by the β of the emitter-follower, allowing the use of low load resistors without sacrificing voltage gain. For cascading stages MOS FET's can be directly coupled up to the output stage, which utilizes the hybrid circuit.

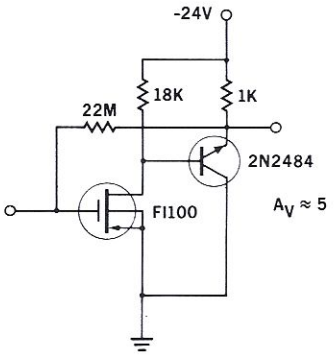


Fig. 5. Self-biased stage with emitter-follower.

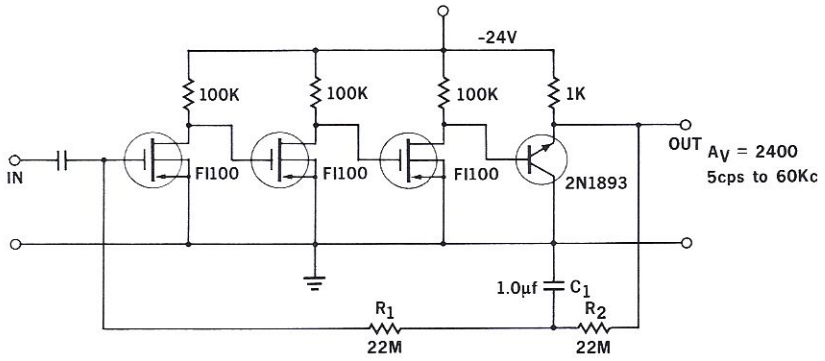


Fig. 6. Multistage self-biased amplifier.

IV. HANDLING PRECAUTIONS

Although the input impedance of the MOS FET is extremely high—in many cases even higher than that of the best vacuum tubes—gate voltage in excess of the rated value is likely to destroy the unit by puncturing the very thin silicon dioxide layer that separates the gate from the semiconductor material. Excessive electrostatic potentials generated by improper handling and testing can damage these units irretrievably. The following precautions must therefore be observed in handling the MOS FET:

1. When working on a breadboard, ground the soldering iron.
2. If possible, contact one of the other leads first before touching the gate lead with the fingers or with ungrounded tools.
3. Protect the gate lead against possible high voltage transients either by electrostatic induction or otherwise.

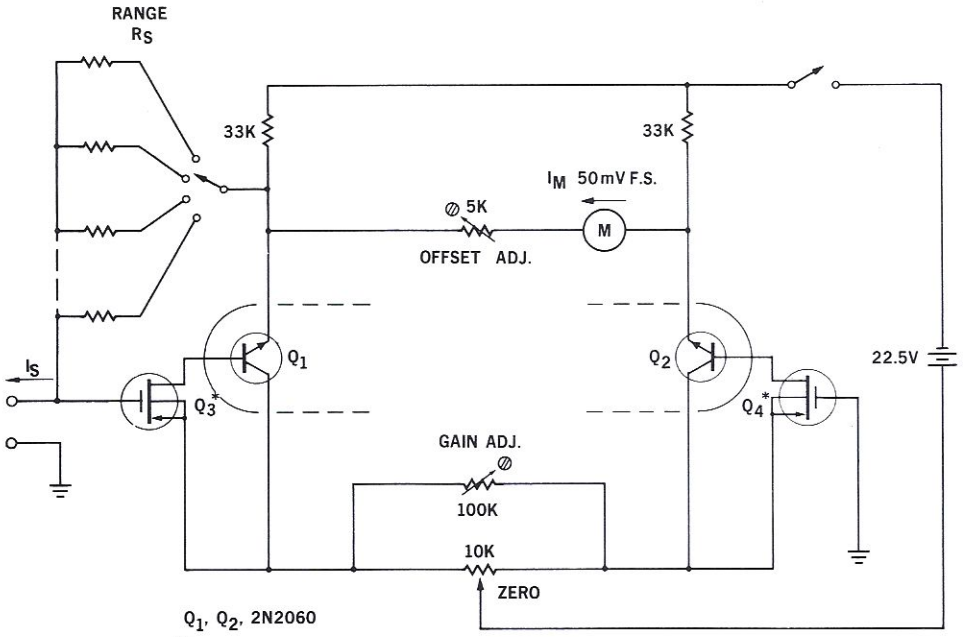
V. APPLICATIONS

1. Multistage self-biased amplifier. Figure 6 shows a multistage DC audio amplifier which has an essentially flat frequency response from 5 cps to 60 Kc and an AC gain of 2400. Each stage adjusts itself to a stable operating level in essentially the same manner as explained for the single-stage amplifiers shown in Figs. 4a and 5. The time constant before equilibrium conditions are reached is necessarily long when very low frequency response is required with bypassed feedback. Bypassing is not essential, but it was used in this case to determine the AC gain possible. R_1 is the DC feedback resistor, which determines the input impedance. The R_2-C_1 time constant, together with the input coupling time constant, determines the low frequency response of the amplifier.

2. Picoammeter. Lacking the leakage current problem of other types of transistors and the "warm-up" time of the vacuum tube, the MOS FET is ideal for measuring extremely small signal currents. The picoammeter in Fig. 7 measures currents of 1 pA full scale using standard-production MOS FET's and the components shown. A signal current I_S produces a change in the emitter current of Q_1 and thus a difference of potential across the meter M.

3. Multivibrators. The MOS FET multivibrator is interesting because of the single-element control of frequency and the large periods that can be obtained. Figures 8a and 8b show two free-running multivibrators. The simple circuit of Fig. 8a will give a period of 15 minutes with a resistor of 10^{12} ohms and a capacitor of 5 pf. The more sophisticated variable-duty-cycle circuit of Fig 8b contains essentially two time constants, one controlling the ON time and the other the OFF time. By this technique duty cycles of tens of thousands to one can be very simply obtained.

The operation of the circuit in Fig. 8b is as follows: Assume Q_1 initially conducting and Q_2 off. The capacitor C will be charging through Q_1, diode D_2, and resistors R_{G2} and R_{L2}. When the voltage at the gate of Q_1 reaches the point where the gate can no longer sustain conduction of Q_1 this device starts to turn off, following the RC time constant.



Input Current I_S for Full Scale Deflection of 10 μA Meter Movement		R_S
1	μA	100 K
0.1	μA	1 M
0.01	μA	10 M
1	mμA	100 M
100	pA	1000 M
10	pA	10 KM
1	pA	100 KM

Fig. 7. Picoammeter

The resulting negative voltage at its drain, and hence at the gate of Q_2, turns Q_2 on, causing the drain of Q_2 to rise toward ground. Diode D_2 is now back-biased, and capacitor C discharges and recharges through R_{L1}, D_1, R_{G1}, and Q_2. Thus the two halves of the duty cycle are set separately by R_{G1} and R_{G2} and can have very wide differential ranges within the leakage limits of D_1 and D_2.

4. Pulse generator. One application of the variable duty cycle obtainable with the MOS FET is in the construction of the simple transistorized pulse generator shown in Fig. 9, which uses MOS FET's to generate the waveform. To obtain high speeds the emitter-followers are added, and the capacitor is charged and discharged through the emitter-followers rather than through the 10 K load resistors of the MOS FET's. Otherwise the operation is similar to that of the circuit in Fig. 8b.

5. Switches and choppers. The input circuit of the transistor is tied to the output circuit by a diode that may be either forward- or reverse-biased; the grid of the vacuum tube is subject to more or less current flow; but the gate of the MOS FET is almost completely isolated from the source-drain circuit. An obvious application of this characteristic is the switch or chopper. As an r-f switch the device is useful to about 10 Mc, as shown by the circuit and graph of Figs. 10 a and b.

As an audio chopper the MOS FET has been used satisfactorily in the circuit of Fig. 11. In this circuit potentiometers supply the chopper with a DC prebias and reduce the AC switching signal from the multivibrator to minimize the very small capacitive spikes. Since there is no offset and no leakage, this type of simple circuit is quite suitable for the switching of signals of under 100 μV.

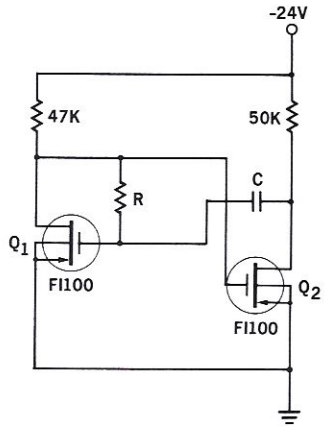


Fig. 8a. Free-running multivibrator.

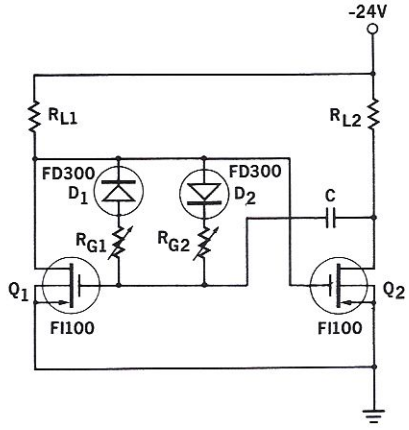


Fig. 8b. Free-running, variable-duty-cycle multivibrator.

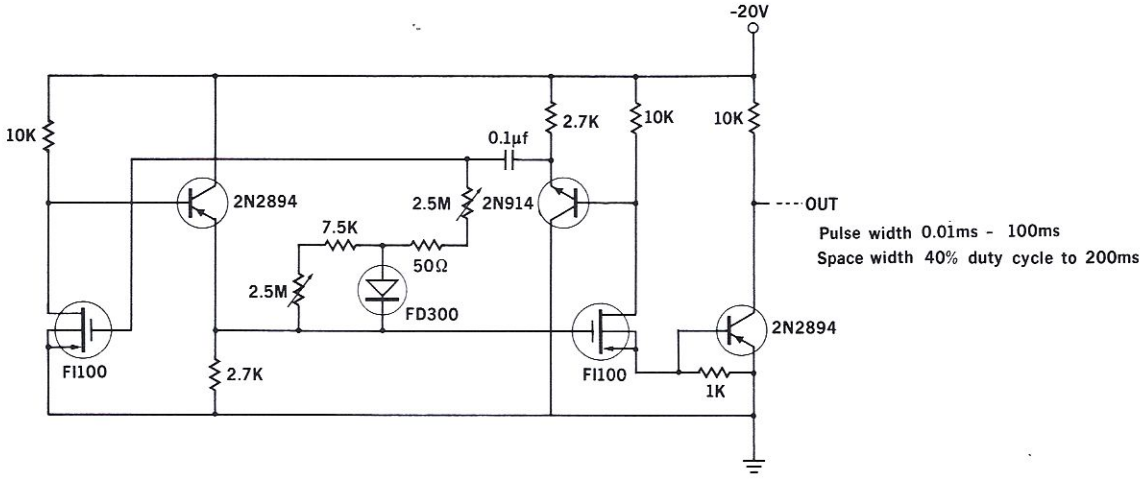


Fig. 9. Pulse generator.

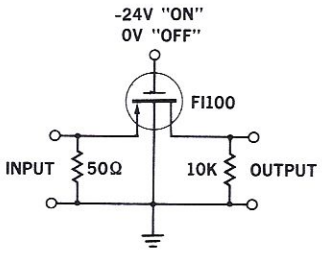


Fig. 10a. The MOST FET as an r-f switch..

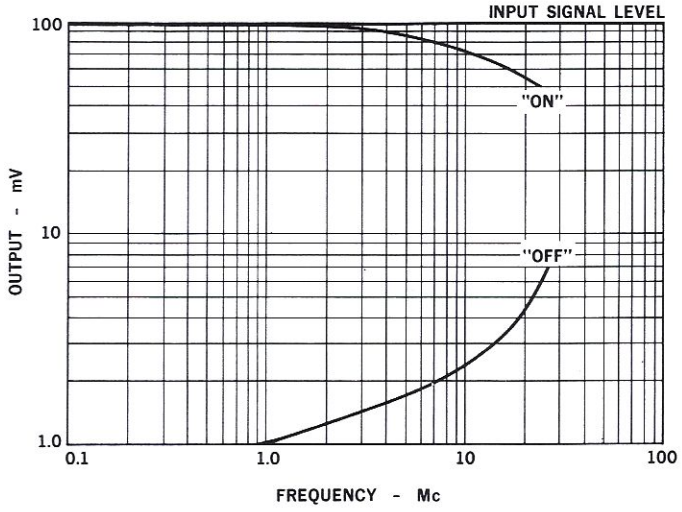


Fig . 10b. Output voltage versus frequency for Fig. 10a circuit.

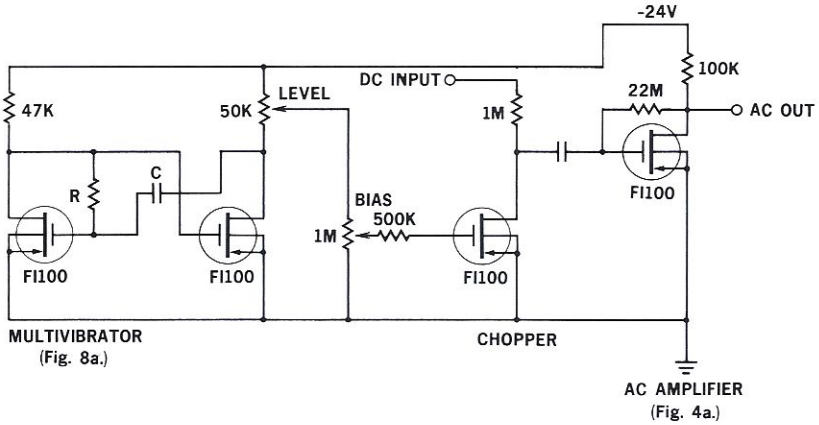


Fig. 11. Chopper for DC amplifier.

6. Voltage-variable attenuators. Although the source is usually held either at the same potential as the base substrate or negative to it, the P-N junction between the two can be forward-biased by more than 100 mV without affecting the operation of the device. This fact suggests the use of the MOS FET as a small-signal voltage-variable attenuator. The curves of Fig. 12 illustrate how the device can be used as a series- or shunt-element small-signal attenuator for frequencies up to 100 Mc. The output capacitance C_{ds} remains nearly constant at approximately 1.5 pf.

Two possible voltage attenuator circuits are shown in Figs. 13a and 13b together with their control curves.

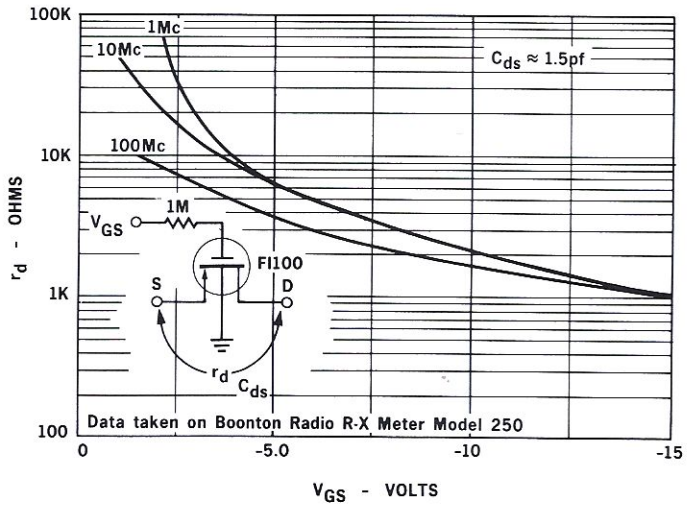


Fig. 12. Curves of drain-to-source resistance versus gate potential for frequencies of 1, 10, and 100 Mc.

7. Wien bridge oscillator. The Wien bridge oscillator (see Fig. 14a for simplified schematic and 14b for complete schematic) demonstrates the use of the MOS FET both as a DC amplifier and as an attenuator. A minimum of components is used by arranging the amplifier circuitry as a DC amplifier using the direct-coupling capabilities of the MOS FET gate. Positive feedback is applied to the top of the frequency-selective network and, unlike the usual Wien bridge circuit, negative feedback is supplied to the bottom of the network by an inverter-amplifier. The amount of negative feedback is controlled by a MOS FET attenuator which obtains its AC signal from an output attenuator and its DC control signal from an output rectifier.

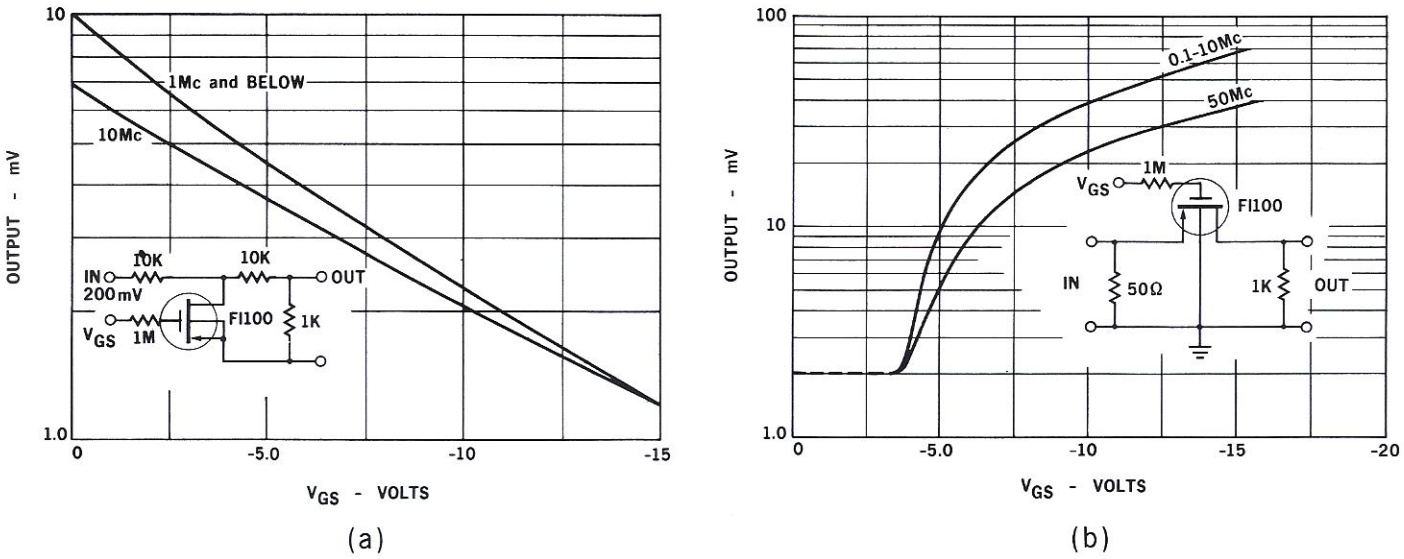


Fig. 13 R-f or video attenuators: (a) shunt and (b) series, and their respective control curves.

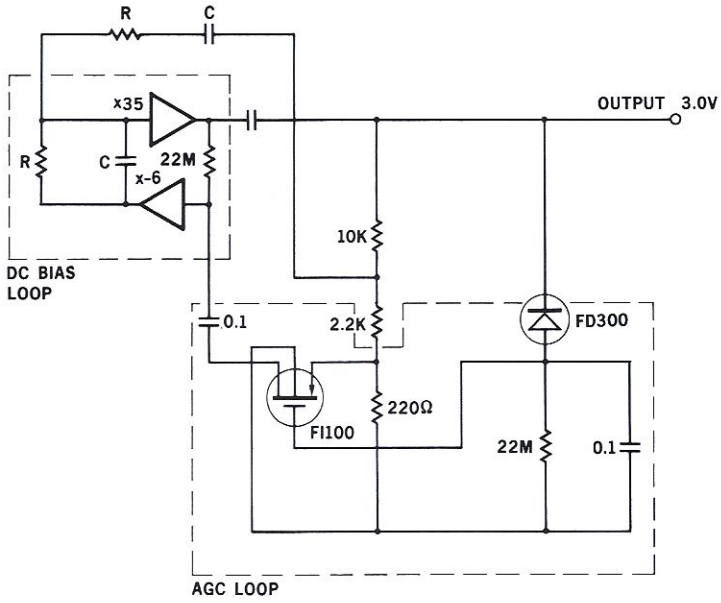


Fig. 14a. Wien bridge oscillator—simplified.

8. Miscellaneous MOS FET applications utilizing the long time constant and high input impedance. The extremely long time constant and high input impedance of the MOS FET can be used in a variety of interesting ways. One of the simplest is the "people detector" of Fig. 15. A human being in the vicinity of the antenna adds capacitance to the input capacitance of the MOS FET, causing a change in gate voltage which is reflected to the output circuit and amplified. The emitter-base junction of the transistor is used as a Zener diode, drawing extremely low currents but still allowing self-bias. This circuit can be used as an alarm since it will easily detect a moving person 10 feet away and is completely passive.

Pulse circuit designers should be interested in the "hold" circuit of Fig. 16. Since the MOS FET input time constant is on the order of several hours, the hold time of the circuit is essentially limited only by the leakage of the charge storage capacitor and the input diode.

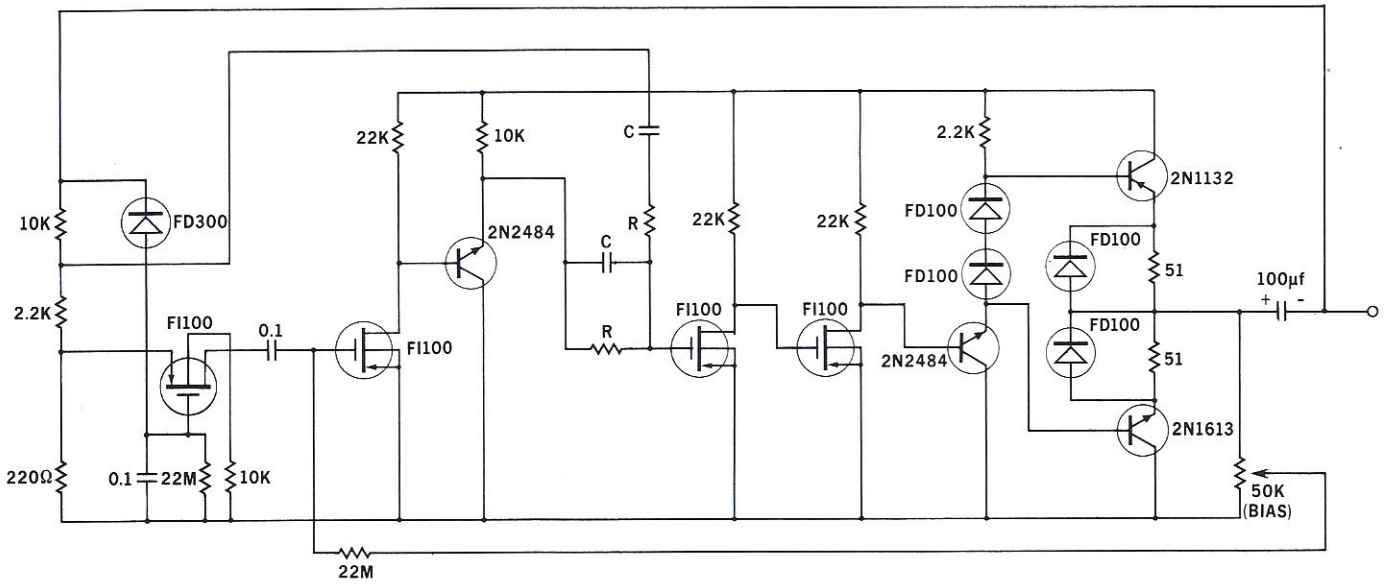


Fig. 14b. Wien bridge oscillator—complete schematic.

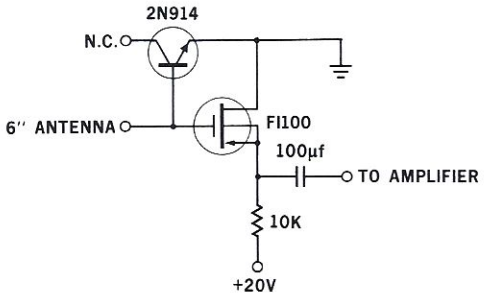


Fig. 15. People detector.

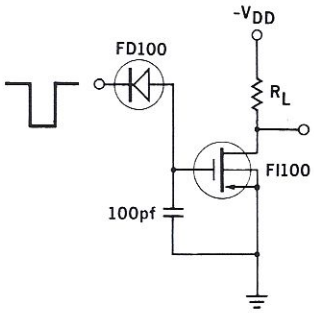


Fig. 16. Pulse "hold" circuit.

A simple circuit for demonstrating the input time constant is shown in Fig. 17. The output current can be set to some value by adjusting the potentiometer at the input and pushing the switch. This current will then remain flowing for several hours with the switch open.

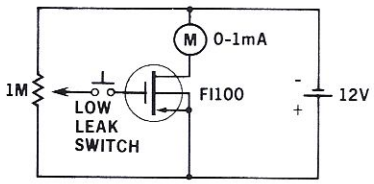


Fig. 17. Input time constant demonstrator.

VI. CONCLUSION

The special properties of the MOS FET (e.g., its spectacularly high input impedance, long time constant, ease of direct coupling, and almost complete isolation of the input circuit from the output) also adapt it to the following applications not covered in this note: ultra linear sweep and integrator, analog amplifier, pulse height analyzer, DC amplifier, staircase generator, electrostatic voltmeter, long-period timer, solid-state electrometer, and others. In addition to the applications that utilize its peculiar properties, it appears that the device will be directly competitive with the junction FET in more conventional circuits.[5, 6]

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ACKNOWLEDGEMENT:

At the outset of the investigation considerable help was provided by the prior work done in the R&D facility at Fairchild. Some of the ideas shown and developed here were originally used or suggested there, notably the pico-ammeter circuit, the multivibrator, and the self-bias concept.

The equivalent circuit was evaluated by B. Barranger. The "people detector" was originated by W. Alexander. R. Shultz provided much encouragement and initiative.

Joe Caponera did much of the testing and breadboarding and developed the pulse generator in Fig. 9.

LIST OF SYMBOLS

C_{ds}	Output capacitance
C_{gd}	Gate-to-drain capacitance
C_{gs}	Gate-to-source (plus gate-to-channel) capacitance
e_{gs}	Gate-to-source signal voltage
I_D	Drain current
r_d	Dynamic drain resistance
R_{GS}	Gate leakage resistance
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_{GST}	Gate threshold voltage
y_{fs}	Gate-to-drain transconductance (g_m)